Technology Related Design of Monolithic Millimeter-Wave Schottky Diode Mixers

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(Invited Paper)

Abstract—**The development of monolithic millimeter-wave Schottky diode mixers based on technological parameters is described. The complete equivalent circuit of the monolithic Schottky diode is calculated taking into account the semiconductor layer structure and the device geometry. This model has been used in a harmonic balanced software for designing monolithic single balanced mixers. In *V*-band a minimum DSB noise figure of 3.3 dB and a minimum conversion loss of 6 dB have been achieved. In *W*-band a minimum DSB noise figure of 4 dB and a minimum conversion loss of 7 dB have been obtained.**

I. Introduction

THE DEVELOPMENT of GaAs millimeter-wave MMIC's is a key factor for the low cost, high volume production and size reduction of millimeter-wave systems. Due to the small dimensions in this frequency range, technologies which allow the monolithic integration of different circuit functions on one chip will be of great advantage. First investigations are aimed at developing monolithic integrated circuits such as mixers for applications in receiver front ends.

A new technology which allows the integration of Schottky diodes (mixer, multiplier) and MESFET's (local oscillator, IF amplifier) on the same chip has been developed [1], [2]. Schottky diode mixers are currently employed in the millimeter-wave frequency range because of their superior performances over MESFET mixers. Because of the MMIC configuration it is not possible to tune the diode matching impedances after the circuit realization, hence a precise equivalent circuit of the diode and a careful analysis of the mixer are required.

An accurate model of the Schottky diode based on the technological parameters is presented in the first part of this paper. The second part is devoted to the mixer analysis which is performed by the harmonic balance technique. In the third part several results of realized monolithic millimeter-wave mixers are given. The desired performances have been already achieved by the first pass design.

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II. Technology and Diode Modeling

The novel technology for the monolithic integration of both planar Schottky diodes and GaAs MESFET's has been described in a previous paper [2]. It includes an n^+ buried layer to reduce the diode series resistance. A schematic cross section of the planar Schottky diode is shown in Fig. 1. The buried n^+ zones are formed by selective implantation into the semi-insulating substrate. The active n layer and a further n^+ layer are deposited by MOCVD. The active layer is used for both the MESFETs and the diodes. The gate contact of the MESFETs and the Schottky diode fingers are recessed simultaneously. The minimum structure size is 0.3 μm. A large signal model of the Schottky diode based on the diode structure has been developed. The equivalent circuit shown in Fig. 2 is composed of linear and non linear elements. Each component is described by an analytical equation taking into account the technological parameters. For the calculations the doping profile in the GaAs layers is assumed to be uniform. A top view of a one finger diode is shown in Fig. 3. L_F is the finger length, W_F the finger width, L_C the distance between ohmic and Schottky contacts and W_C the ohmic contact width. These notations are used in the following model description.

A. Parasitic Capacitance C_P

The parasitic capacitance C_P is a linear element and represents the coupling capacitance between the ohmic and Schottky contact metallizations. It is composed of four parts:

$$C_P = C_1 + C_2 + C_3 + C_4. \quad (1)$$

The capacitances C_1, C_2 and C_3 are given by (2) for two coupled lines after [3]:

$$C_i = \epsilon_0(1 + \epsilon_R)W_i K(\sqrt{1 - k_i^2})/K(k_i) \qquad i = 1, 2, 3 \quad (2)$$

where

- ϵ_0 is the permittivity in vacuum
- ϵ_R is the dielectric constant of the semiconductor material
- W_i is the coupling length
- $K(k_i)$ is the complete elliptic integral of the first kind

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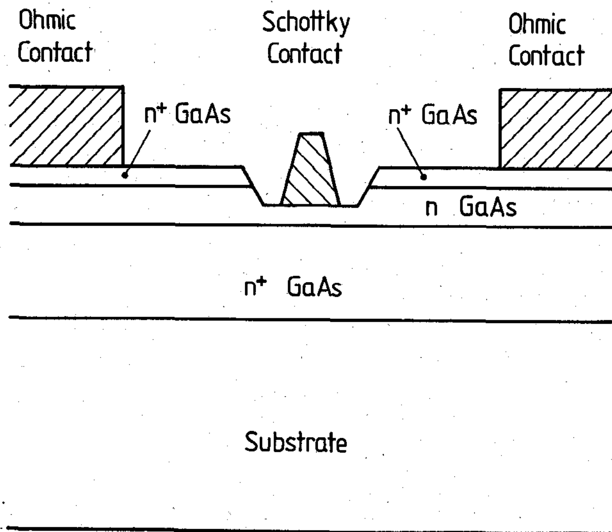
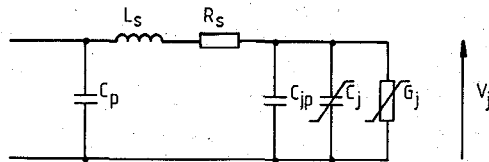


Fig. 1. Schematic cross section of the planar Schottky diode.



$$C_j = \frac{C_{jo}}{\left(1 - \frac{V_j}{V_{bi}}\right)^{\gamma}}$$

$$G_j = \frac{qI_o}{nkT} \exp\left(\frac{qV_j}{nkT}\right)$$

Fig. 2. Large signal equivalent circuit of the Schottky diode.

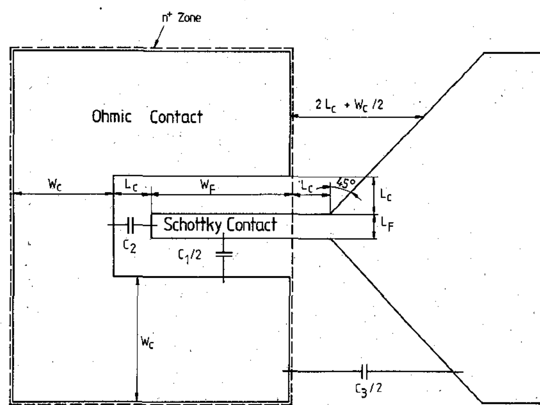


Fig. 3. Top view of a one finger diode.

k_i is a parameter depending on the geometry of the coupling lines

In order to consider the corner capacitances at the end of the finger, effective finger coupling lengths have been defined for the finger width W_F as $W_{Fe} = W_F + L_C/2$ and for the finger length L_F as $L_{Fe} = L_F + L_C$.

C_1 is the coupling capacitance along the Schottky finger width. In (2) $W_1 = 2W_{Fe}$ and $k_1^2 = L_C/(L_C + L_F)$,

C_2 is the coupling capacitance at the end of the Schottky finger along the finger length. In (2) $W_2 = L_{Fe}$ and $k_2^2 = (2W_C + L_C)L_C/(W_C + L_C)^2$,

C_3 is the coupling capacitance between the Schottky lead and the ohmic contact (see Fig. 3). In this case a mean gap of $2L_C + W_C/2$ and a line width of $W_C + L_C + W_F$ are taken, then in (2) $W_3 = 2W_C + L_C$ and $k_3^2 = [2(W_C + L_C + W_F) + (2L_C + W_C/2)]\,[2L_C + W_C/2]/[(W_C + L_C + W_F) + (2L_C + W_C/2)]^2$.

The capacitance C_4 in (1) is the parallel plate capacitance between the metallizations of the Schottky and ohmic contacts and is described by the expression (3)

$$C_4 = \epsilon_0 \epsilon_{RP} T_m (2W_{Fe} + L_{Fe})/L_C \quad (3)$$

ϵ_{RP} is the dielectric constant of the passivation layer T_m is the thickness of the Schottky metal.

B. Junction Capacitance

The thickness of the depleted region under the Schottky contact is given by the resolution of the Poisson equation. Assuming abrupt doping densities the parallel plate capacitance C_{jpp} is expressed by

$$C_{jpp} = (qN_D \epsilon_0 \epsilon_R / 2(V_{bi} - V_j))^{1/2} L_F W_F \quad (4)$$

when the depleted region is only in the n GaAs layer and by

$$C_{jpp} = \epsilon_0 \epsilon_R (2\epsilon_0 \epsilon_R (V_{bi} - V_j)/qN_{DP} + (1 - N_D/N_{DP}) T_n^2)^{-1/2} L_F W_F \quad (5)$$

when the depleted region has reached the n^+ buried layer. In (4) and (5) N_D and N_{DP} are respectively the doping densities of the n layer and the n^+ buried layer, V_{bi} is the built-in voltage of the Schottky contact, V_j is the junction voltage, T_n is the thickness of the GaAs n layer under the contact and q is the electron charge.

The capacitance of small area Schottky diodes is strongly affected by the edge effects. Assuming that the depleted region at the edge of the contact is a quarter of a circle [4], the fringing capacitance C_{jF} is given by (6).

$$C_{jF} = \pi \epsilon_0 \epsilon_R (2W_F + L_F)/2 \quad (6)$$

C_{jF} is voltage independent.

The total junction capacitance C_{jT} is given by

$$C_{jT} = C_{jpp} + C_{jF}. \quad (7)$$

In Fig. 2 the total junction capacitance is described by

$$C_{jT} = C_j + C_{jP} \quad (8)$$

with

$$C_j = C_{j0}/(1 - V_j/V_{bi})^{\gamma}. \quad (9)$$

A first solution can be formed by assuming that the depleted region is only in the n layer. In this case

$$C_{jP} = C_{jF}, \quad \gamma = 0.5 \quad \text{and}$$

$$C_{j0} = (qN_D \epsilon_0 \epsilon_R / 2V_{bi})^{1/2} L_F W_F.$$

To take into account that the depleted region can reach the n^+ buried layer, the values of C_{jP}, C_{j0} and γ in (8) and (9) have been adjusted to fit (7). An example is given in Fig. 4.

C. Parasitic Resistance R_S

The parasitic resistance R_S is composed of the ohmic contact resistance R_O, the resistance between the Schottky and ohmic contacts R_{BC}, the resistance under the junction R_G and the resistance of the finger metal R_F.

$$R_S = R_O + R_{BC} + R_G + R_F. \tag{10}$$

According to [5] the ohmic contact resistance is given by

$$R_O = \sqrt{R'_\square R_C}\,[\coth(\sqrt{R'_\square / R_C}\, W_C)] / (2W_{Fe} + L_{Fe}) \tag{11}$$

where

- $R'_\square$ is the sheet resistance of the semiconductor layers under the ohmic contact (n^+ ion implanted layer, n active layer and n^+ cap layer) in $\Omega/\square$
- R_C is the specific contact resistance in Ωm^2

W_{Fe} and L_{Fe} are the effective lengths defined in part A of this paragraph.

The resistance between Schottky and ohmic contacts is simply expressed by

$$R_{BC} = R'_\square L_C / (2W_{Fe} + L_{Fe}). \tag{12}$$

For the computation of the resistance R_G under the Schottky contact, the distributed network in Fig. 5 is used. The length ΔL_F is infinitesimal small:

$$R_1 = \Delta L_F R'_\square / 2W_F \tag{13}$$

is the resistance in the n^+ buried layer ($R_\square$ is the sheet resistance of this layer)

$$R_2 = \rho(T_n - T_D)/W_F \Delta L_F \tag{14}$$

is the resistance in the n layer where T_D is the thickness of the depleted region and $\rho = 1/\text{quN}_\text{D}$ is the resistivity of the n layer.

$$C_2 = C_{jpp}\, \Delta L_F / L_F \tag{15}$$

is the parallel plate capacitance of the depleted region, C_{jpp} is defined by (4) and (5).

The chain matrix of one cell with length ΔL_F is determined and the chain matrix (C) of the complete circuit is calculated. The impedance Z_G under the gate is given by

$$Z_G = V_1 / 2I_1 \tag{16}$$

for $V_1 = V_2$ and $I_1 = -I_2$.

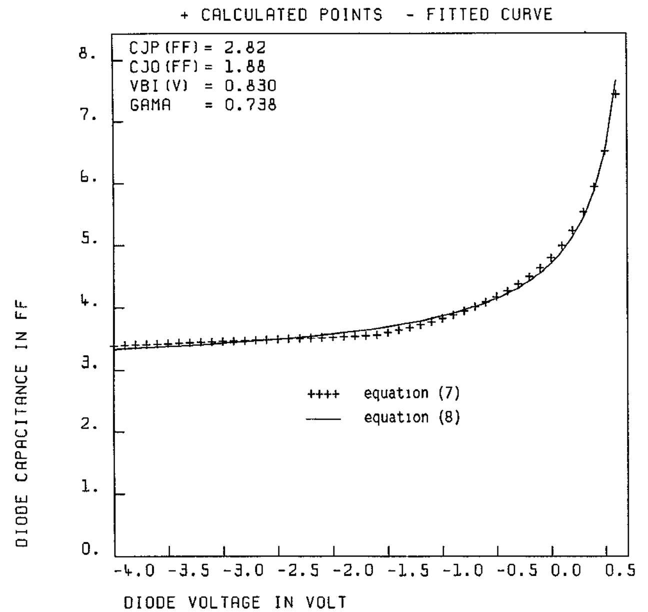
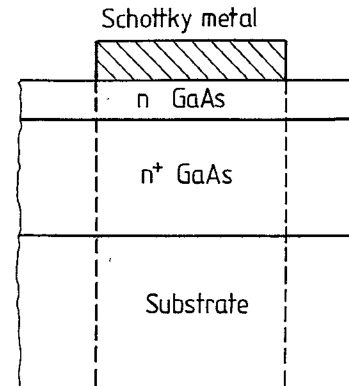


Fig. 4. Calculated junction capacitance versus diode voltage for a 0.3 × 5 μm^2 diode.



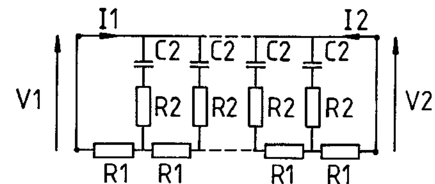


Fig. 5. Distributed network model for the calculation of the impedance under the Schottky contact.

From the chain matrix

$$Z_G = C_{12}/2(C_{11} - 1), \tag{17}$$

C_{11} and C_{12} are the elements of the chain matrix (C).

The resistance R_G is the real part of the impedance Z_G.

The resistance R_F of the Schottky metal is described by the well-known relation [8]

$$R_F = \rho_F W_F / 3L_F T_m \tag{18}$$

where ρ_F is the resistivity of the metal. The skin effect in the Schottky metal is taken into account by determining

an equivalent thickness T_{meq} [6]

$$T_{meq} = \delta(1 - \exp(-T_m/\delta)) \quad (19)$$

where $\delta = 1/\sqrt{\pi\mu\sigma f}$ is the skin depth, μ the permeability in vacuum, σ the conductivity and f the frequency.

The skin effect in the semiconductor is neglected due to the small thickness of the n^+ buried layer (0.55 μm) compared to the skin depth. At 100 GHz the skin depth in GaAs layer with a doping density of 2.10^{18} cm^{-3} is approximately 5 μm. From the computation the resistance R_S is voltage dependent. In the model we assume a constant value calculated for a junction voltage equal to zero.

D. Junction Conductance

At room temperature the *I-V* characteristic of the Schottky junction is well described by the thermionic emission theory [7]:

$$I = I_0(\exp(qV_j/nkT) - 1) \quad (20)$$

$$I_0 = A^* T^2 S \exp(-qV_b/nkT) \quad (21)$$

where

- I_0 is the reverse saturation current,
- A^* the modified Richardson constant,
- V_b the barrier height,
- T the temperature,
- S the contact area,
- n the ideality factor.

The junction conductance G_j is the derivative of the current:

$$G_j = (qI_0/nkT)\exp(qV_j/nkT) \quad (22)$$

In (22) the ideality factor n and the reverse saturation current I_0 are to determine. These two parameters are depending on the technology. They can be measured using the characteristic Log (I) versus the diode voltage as shown in Fig. 6, [8]. The ideality factor is obtained by a linear regression for small current values. The extrapolation of the obtained straight line to a zero diode voltage gives the reverse saturation current I_0. The dc resistance R_S is evaluated by the difference between a measured point and the straight line for high current level.

From (21) the knowledge of I_0 allows the evaluation of the barrier height V_b and then the built in potential V_{bi} as

$$V_{bi} = V_b - (kT/q)\ln(N_C/N_D) \quad (23)$$

where N_C is the density of states in the conduction band of the n layer. The built-in potential is required for (4), (5), and (9).

For a mature technology the ideality factor and the built-in potential are reproducible, so it is possible to calculate the conductance G_j of any diode from (22) and (21).

E. Parasitic Inductance L_S

Due to the planar configuration the parasitic inductance L_S is assumed to be zero.

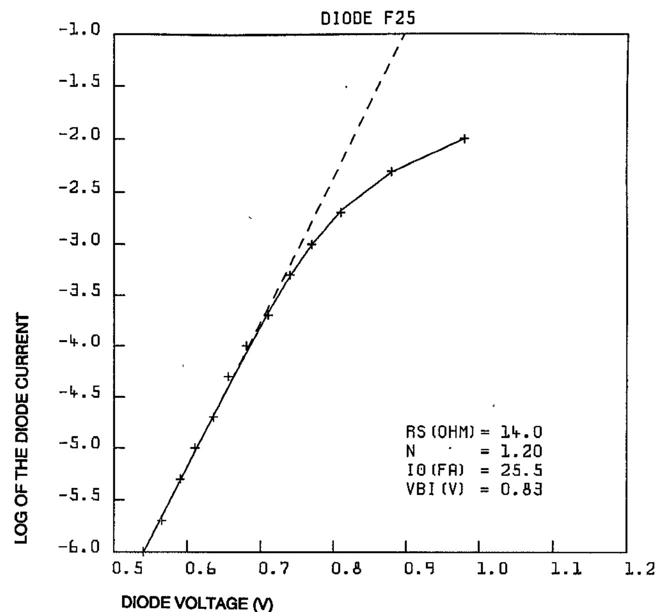


Fig. 6. Diode *I-V* characteristic. The finger area is 0.3 μm × 5 μm. + + + + measurement; --------- slope at low current giving the ideality factor n; —— characteristic calculated with the parameters R_S, n and I_0 extracted; from the measurements.

TABLE I
COMPARISON BETWEEN CALCULATED AND MEASURED DIODE SERIES RESISTANCES AND CAPACITANCES

Diode Type	Number of Fingers	Finger Dimensions	R_S Calculated	R_S Measured	C_T Calculated	C_T Measured
F01	3	0.3 × 4.0	5.2	6.1	20.	19.
F09	3	0.5 × 4.0	4.7	5.0	24.	22.-26.
F15	3	1.0 × 4.0	4.2	3.2	35.	32.-37.
F25	1	0.3 × 5.0	13.6	14.0	8.	9.

Finger dimensions: length x width in μm; R_S: diode resistance in ohm; C_T: diode capacitance in *fF*.

Different diodes have been fabricated and characterized to study the process technology. The measured series resistance R_S and diode capacitance $C_T = C_{jT} + C_p$ are in good agreement with the calculated values as shown in Table I. C_{jT} is defined by (7) or (8) and C_p by (1). A diode with n fingers is considered as the parallel connection of n one finger diodes.

The mean values of the built-in potential V_{bi} and the ideality factor are found to be 0.83 V and 1.22, respectively.

III. MIXER ANALYSIS

The mixer design is based on the following steps:

diode nonlinear model using the previous described large signal equivalent circuit;

harmonic balance analysis of the diode as a single ended mixer to determine the optimum embedding impedances and for the choice of the appropriate diode geometry;

embedding impedances synthesization;

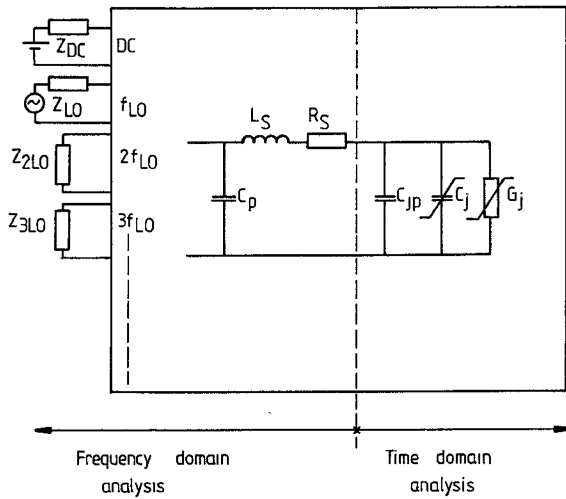


Fig. 7. Large signal equivalent circuit of the mixer.

complete circuit design (single ended mixer or balanced mixer).

A. Single Ended Diode Mixer Analysis

The developed diode model is implemented in a large signal analysis program based on the harmonic balance technique. This CAD program uses the multiple reflection algorithm as described in [9], [10]. The large signal equivalent circuit of the mixer is represented in Fig. 7. It is assumed that the RF excitation is negligibly small compared to the local oscillator so the diode is first analyzed under LO excitation only. The nonlinear elements are treated in the time domain. The parasitic elements and the embedding impedances are analyzed in the frequency domain. So the circuit is divided into a non-linear subcircuit and a linear subcircuit. The voltage waveform at the junction between these two subcircuits is matched to give the same currents in both the time domain analysis and the frequency domain analysis. This time waveforms of the junction capacitance and conductance are formed from the voltage waveform solution of the large signal analysis. The Fourier coefficients of the junction conductance and capacitance are computed for performing the small signal analysis without further consideration of the LO excitation (Fig. 8) [9], [10]. The result is expressed by a multiport conversion matrix considering all sideband frequencies of the form $nf_{LO} \pm f_{IF}$ with $n = 1, 2, \cdots$. By taking into account the embedding network this matrix is reduced to a two port conversion matrix with RF and IF signals.

A noise analysis is also implemented in the CAD program. For this purpose the noise equivalent circuit of Fig. 9 is considered [9], [10]. Two noise sources are taken into account:

$\overline{i_S^2}$: the shot noise due to the junction current depending on the LO waveform;

$\overline{v_t^2}$: the thermal noise due to the parasitic resistance R_S.

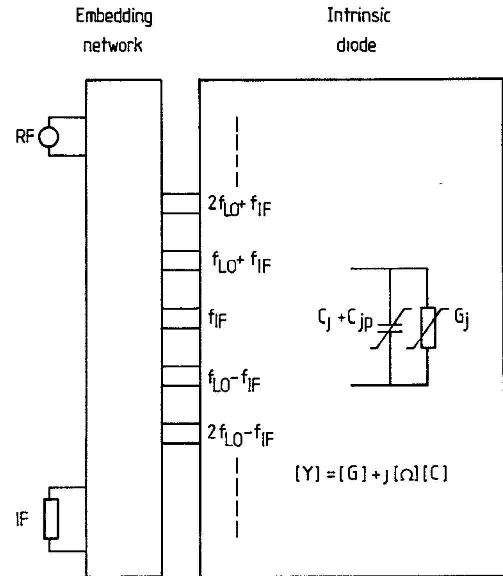


Fig. 8. Small signal equivalent circuit of the mixer.

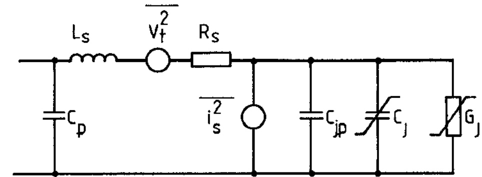


Fig. 9. Noise equivalent circuit of the diode. Shot noise source $\overline{i_S^2} = 2qIB$. Thermal noise source $\overline{v_t^2} = 4kTR_SB$.

The excess noise is not considered. At room temperature it represents a small part of the entire noise [9] but is increasing with the LO power level [11]. For millimeter-wave applications a design goal is to reduce the request of the LO power, so the excess noise can be neglected. Therefore it is possible to simply introduce the excess noise in the thermal noise correlation matrix to derive a complete noise analysis [11].

The CAD analysis program allows the optimization of the RF and image frequency embedding impedances for obtaining the minimum noise figure or the minimum conversion loss.

For the validation of the program a hybrid single ended mixer using a 3 fingers diode was realized. Each finger of the diode has an area of $0.3 \times 4\ \mu m^2$. The simulated conversion loss is in good agreement with the measured one as shown in Fig. 10(a). The simulated double side band noise figure is slightly lower than the measured one for LO power level under 6 dBm. This can be due to excess noise or AM noise from the local oscillator. For LO power level greater than 6 dBm the excess noise becomes important and the difference between measurement and simulation is greater.

B. Balanced Mixer Analysis

An equivalent circuit of a single balanced mixer is represented in Fig. 11. First the Schottky diode is analyzed

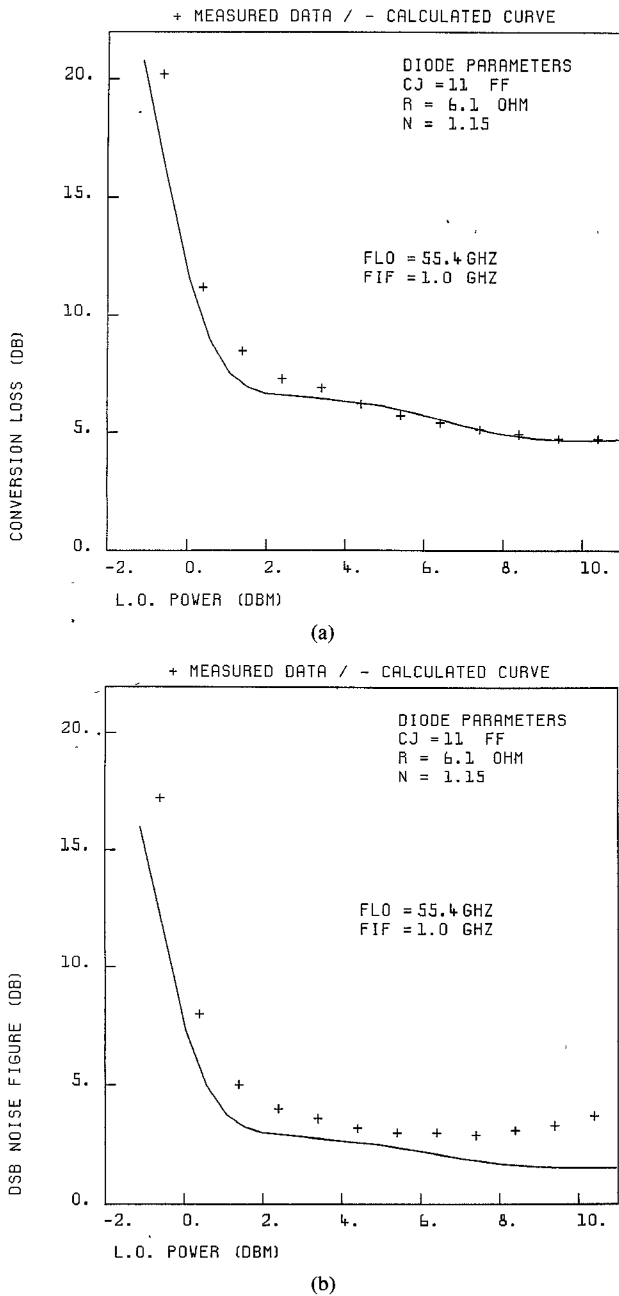


Fig. 10. Measurement results of a single ended mixer realized with a 3 fingers diode. (a) Conversion loss. (b) Noise figure.

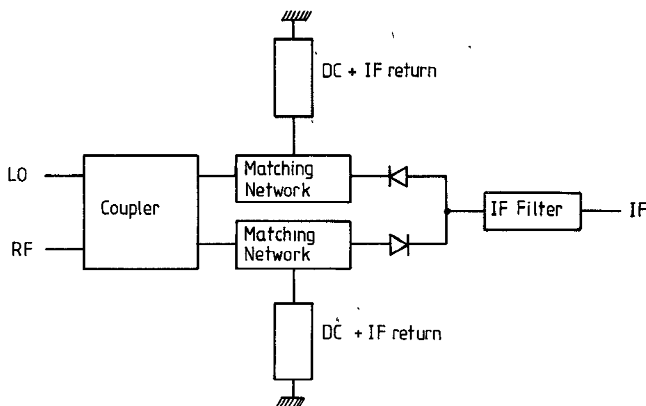


Fig. 11. Schematic equivalent circuit of a single balanced mixer.

in a single ended mixer configuration as described in part A. The matching impedances for the RF signal and the image frequency are optimized for satisfying the design goal. Knowing these impedances the embedding network of the diode is determined and the complete single balanced mixer circuit is designed. The in house software to calculate microstrip discontinuities and radial stubs has been improved for the millimeter-wave frequency range. A fine linear optimization of the diode matching network is made by considering the entire single balanced mixer circuit. From this analysis the IF impedance can be calculated to realize an optimum matching to an IF amplifier.

IV. Experimental Results

We have realized several MMIC single balanced mixers in the *V* and *W*-band frequency ranges. For all these mixers the diode equivalent circuit was calculated from the model described in part II and the mixer analysis was performed as in part III of this paper. Our design goals were minimum noise figure and minimum LO power request. The choice of the diode area was dictated by the power request and the impedance level. The embedding impedances of the RF and image frequencies have been optimized for minimum noise figure.

A. V-Band Mixer

The results of a first 60 GHz monolithic mixer are reported in [2], [12]. A DSB noise figure of 3.3 dB combined with 6 dB conversion loss in self bias operation has been achieved. The LO power is 6.5 dBm at 55.4 GHz. The IF frequency is 4.1 GHz. The chip area is 2.5 × 4 mm^2. The mixer diode size is only 0.3 × 5 μm^2 in order to drive the mixer with minimum LO power.

A new mixer for 51 GHz was designed with a Lange coupler. The aim was to reduce the chip area. A diode size of 0.5 × 5 μm^2 was used in this case. The mixer circuit is shown in Fig. 12. The configuration is the same as that of the previous 60 GHz mixer. The mixer is designed for self bias operation. The circuit comprises two via holes for dc and IF returns. The chip area is 2 × 3 mm^2, this is a reduction of 40% compared to the previous mixer. The measured noise figure and conversion loss versus LO power are shown in Fig. 13(a). A DSB noise figure of 4.7 dB associated with a conversion loss of 6.1 dB at 51.4 GHz and 7.9 dB at 59.4 GHz is achieved. The LO power is 10 dBm at 55.4 GHz for these performances. In figure 13b the conversion loss and the DSB noise figure are given for an IF frequency range from 3.5 GHz to 5.5 GHz. In this case the conversion loss is between 7.1 dB and 8.3 dB for the upper sideband and between 6.1 dB and 7.1 dB for the lower sideband whereas the DSB noise figure varies between 4.7 dB and 5.8 dB.

B. W-Band Mixer

A monolithic 94 GHz mixer was reported in [13]. Fig. 14 shows the mixer circuit. The DSB noise figure and the conversion loss versus LO power and IF frequency are

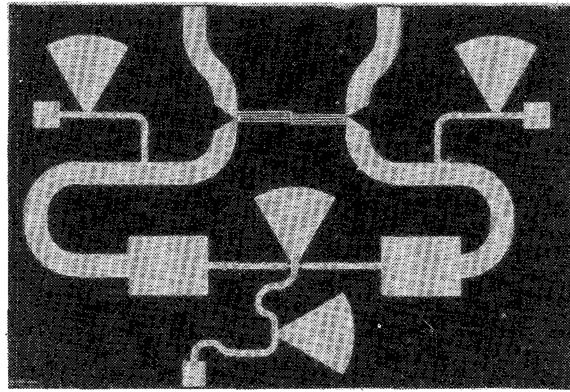


Fig. 12. *V*-band mixer.

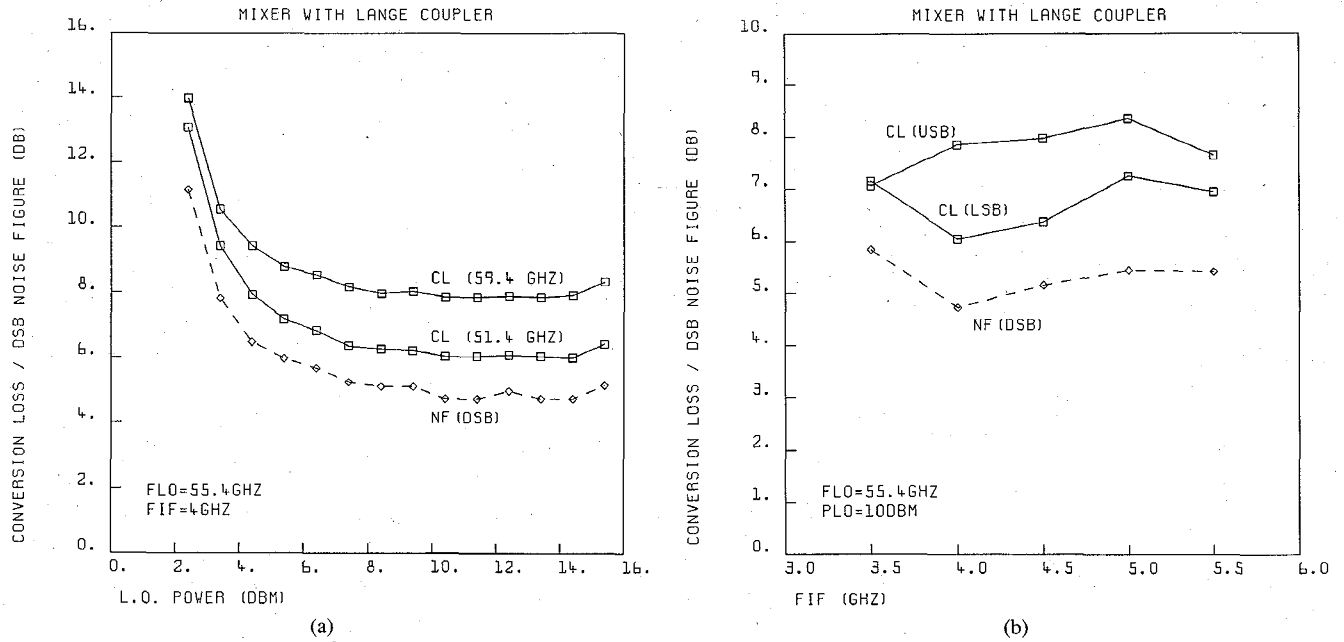


Fig. 13. DSB noise figure and conversion loss versus (a) LO power and (b) IF frequency for the mixer from Fig. 12.

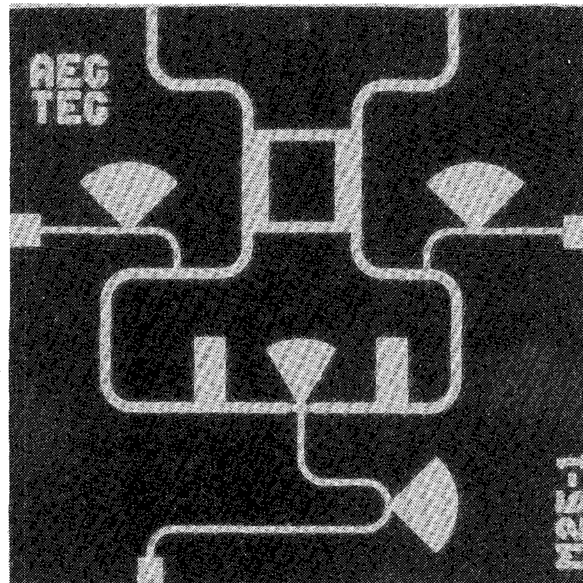


Fig. 14. W-band mixer.

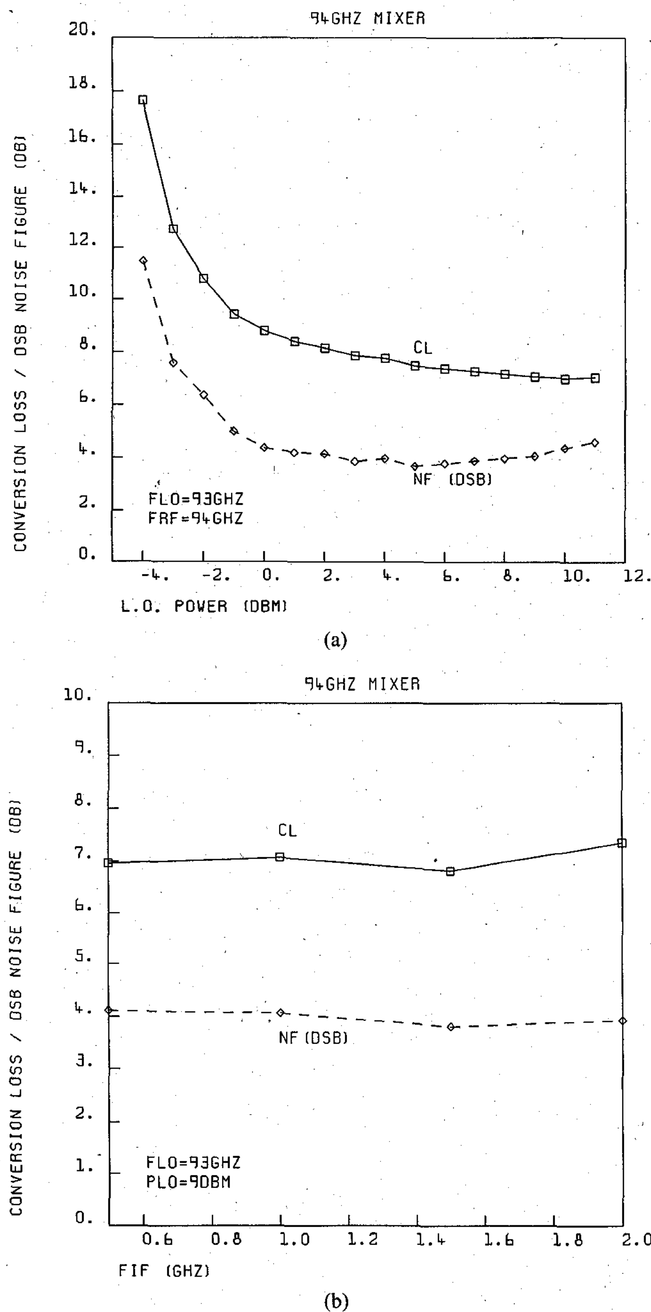


Fig. 15. DSB noise figure and conversion loss versus (a) LO power and (b) IF frequency for the mixer from Fig. 14.

represented in Fig. 15. A DSB noise figure of 4 dB associated with a conversion loss of 7.5 dB has been measured in self bias operation. In this case the LO power is 5 dBm at 93 GHz. The IF frequency is 1 GHz. The Schottky diode area is $0.3 \times 5\ \mu m^2$. The chip size is $2 \times 2\ mm^2$. This mixer shows a very low LO power request.

V. Conclusion

For the design of monolithic Schottky diode mixers a large signal equivalent circuit of the diode based on the technological parameters was developed. This model was implemented in a harmonic balance CAD software for analyzing the mixer circuit. Several mixers in the millimeter-wave frequency range have been designed. The experimental results are in good agreement with the design goals: low noise and conversion loss, minimum LO power request. The presented results are all obtained after the first pass design and prove the validity of the diode equivalent circuit and the design concept. Furthermore the design method is directly applicable to investigate the influence of the technological parameters on the mixer performances. Especially it is possible to predict the mixer performances for microwave applications using a technology without n^+ buried layer.

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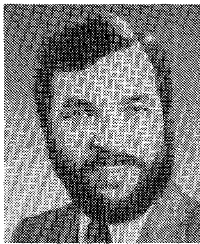

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